and further in view of U.S. Patent 6,074,479 to Adachi et al. and Wolf et al. (Vol. 1). Claims 4 and 5 have been canceled by the Amendment filed October 15, 2003. Accordingly, this rejection is moot as to claims 4 and 5. Applicants respectfully traverse these rejections.

Applicants respectfully submit that one of ordinary skill in the art would not have been motivated by the disclosures of Yamamoto and Sato to employ a method of producing an SOI wafer by bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation, delaminating the bonded wafer, and subjecting the delaminated wafer, in an atmosphere containing hydrogen or argon, to both a heat treatment utilizing a rapid heating/rapid cooling apparatus to improve the surface roughness of short periods of the SOI layer and a heat treatment utilizing a batch processing type furnace to improve the surface roughness of long periods of the SOI layer, as claimed in independent claim 1. Applicants further submit that one of ordinary skill in the art would not have been motivated by the disclosures of Yamamoto, Sato, Adachi and Wolf to employ a method of producing an SOI by bonding a base wafer and a bond wafer, which is selected from an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on surface are reduced, having a micro bubble layer formed by gas ion implantation, delaminating the bonded wafer, and subjecting the delaminated wafer to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace, as claimed in independent claim 3. Nor would such a person have had any reasonable expectation that such methods could be successfully employed.

I. Background of the Invention

Silicon on insulator (SOI) wafers and the methods for making them are of great importance for the semiconductor industry. Methods that can produce SOI wafers at low cost and with high quality are of particular importance for the commercial manufacture of

semiconductor devices. The most desirable SOI wafers are those with good electronic and surface roughness characteristics.

One representative method of producing SOI wafers is the SMART CUT METHOD®. The SMART CUT METHOD® includes the steps of bonding a wafer implanted with hydrogen or other ions and then delaminating the wafer to produce an SOI wafer. This method is a technique for producing an SOI wafer, in which an oxide layer is formed on at least one of two silicon wafers, hydrogen ions or rare gas ions are implanted into the top surface of one wafer to form a micro bubble –enclosed—layer. The ion-implanted surface of the wafer is then bonded to the other silicon wafer via the oxide layer, and the wafers are subjected to a delamination heat treatment to delaminate one of the wafers as a thin film at the micro bubble layer as a cleavage plane. The other wafer is then subjected to a bonding heat treatment. By this process, it is possible to obtain an SOI wafer in which an SOI layer is firmly bonded on the silicon wafer. See Specification, page 1, line 24 - page 2, line 20.

However, the SOI layer surface after delamination at the micro bubble layer has higher surface roughness when compared with a mirror-polished wafer used for usual device production. See Specification, page 2, lines 21-26. The SOI wafer having a higher surface roughness cannot be used for semiconductor device production without improving the surface roughness. Touch polishing is usually performed to improve the surface roughness of the SOI wafer. See Specification, page 2, line 26 - page 3, line 4. Unfortunately, because the SOI layer is extremely thin, polishing may result in significant variations in SOI layer thickness due to the differing amounts of SOI layer removed as surface roughness is improved. See Specification, page 3, lines 5-9.

Thus, the semiconductor industry was presented with the problem of improving surface roughness after delamination without polishing the SOI wafer. One possibility for

improving surface roughness of the SOI wafer was by performing a heat treatment of the SOI layer surface immediately after the delamination. See Specification, page 3, lines 10-13.

There are known methods for improving surface roughness by performing a heat treatment of the SOI layer surface immediately after the delamination. In one such process, a bonding heat treatment was performed in order to strengthen the bond between a support substrate and a single crystal silicon thin film. The bonding heat treatment was followed by another heat treatment, which was performed at a temperature in the range of 1000-1300°C for 10 minutes to 5 hours in a hydrogen atmosphere. See Specification, page 3, lines 14-22. Thus, it was known to reduce surface roughness by subjecting a hydrogen delaminated SOI wafer to hydrogen annealing. Hydrogen annealing, for tens of seconds to several tens of minutes, is generally performed in a batch processing type furnace. See Specification, page 5, lines 8-18.

Although a batch processing furnace enables a heat treatment of a large number of wafers over a long period one time, improving the surface roughness of SOI wafers by hydrogen annealing causes other detrimental effects on wafer quality. For example, if a single crystal silicon thin film SOI layer is formed from a wafer produced by the Czochralski method (CZ method) and has a small thickness of about 0.5 μm or less, hydrogen annealing causes a buried oxide layer is etched by hydrogen gas penetrated through COP (Crystal Originated Particle, a void-like grown-in defect). See Specification, page 4, lines 8-20. Other known atmospheres for heat treatments to improve surface roughness, such as argon, also cannot obviate the problem of etching through COP. See Specification, page 4, lines 21-25. Thus, CZ wafers include crystal defects called COPs introduced therein during the crystal growth. If such a CZ wafer is used as a bond wafer to form an active layer (SOI layer), the COPs penetrate the SOI layer and form pinholes to markedly degrade electric characteristics.

See Specification, page 5, lines 1-7. This is particularly problematic for extremely thin SOI layers, such as those employed in recently developed devices.

Hydrogen annealing is only one method that may be used to improve surface roughness. In addition, a heat treatment for improving surface roughness can be performed by any one of the known short time annealing processes, such as rapid thermal annealing (RTA) or by plasma annealing. See Specification, page 5, lines 8-18. From a manufacturing standpoint, the short time annealing processes, during which only a single wafer may be processed at any given time, are undesirable because they greatly increase manufacturing time and costs.

RTA was considered a promising alternative for improving surface roughness, since RTA uses a rapid heating/rapid cooling apparatus and can be performed within an extremely short period of time. See Specification, page 5, lines 19-22. Because RTA could be performed quickly, it was thought that the buried oxide layer would not be etched and, thus, COPs in the SOI layer could be eliminated. See Specification, page 5, lines 22-27. However, RTA is a single wafer process and, in fact, lowers production efficiency and increases the production costs. See Specification, page 6, lines 1-23.

When Applicants studied the improvement of the surface roughness of SOI wafer by RTA, they discovered that only short period components of surface roughness were improved to a level comparable to that of the mirror-polished wafers usually used for device production. See Specification, page 6, lines 1-7. The long period components were still very much inferior to those of the mirror-polished wafers. See Specification, page 6, 7-9. Applicants further discovered that in order to improve the long period components of surface roughness by RTA, high temperatures and long periods of time were required. See Specification, page 6, lines 10-17.

Applicants decided to investigate alternative ways to improve both the short and long period components of SOI wafer surface roughness without etching the buried oxide layer or introducing COPs. The solutions Applicants chose to pursue were twofold. First, Applicants pursued the claimed method of employing two consecutive heat treatments of the delaminated wafer under either hydrogen or inert atmosphere. Second, Applicants pursued the claimed method of subjecting a wafer having a bonded portion that may be delaminated from an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on surface are reduced, to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace.

II. The Claimed Invention

The Applicants have developed, for the first time, methods for improving surface roughness over both the short period and the long period of an SOI layer surface, which has been delaminated by the hydrogen ion delamination method without polishing. For the first time, Applicants were able to secure the thickness uniformity of the SOI layer, as well as efficiently produce SOI wafers free from generation of pits due to COPs in SOI layers. In addition, Applicants were able to accomplish these results with increased "throughput" and efficiency.

In particular, Applicants have unexpectedly found that an SOI wafer having improved surface roughness, uniform SOI layer thickness and being substantially free from COP-induced pits can be achieved by the method of independent claim 1. That is, Applicants found that an SOI wafer having improved surface roughness, uniform SOI layer thickness and being substantially free from COP-induced pits could be produced by the combination of:

- bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation;
- delaminating a wafer having an SOI layer at the micro bubble layer as a border, and

- subjecting the wafer having an SOI layer, in an atmosphere containing hydrogen or argon, to both a heat treatment utilizing a rapid heating/rapid cooling apparatus to improve the surface roughness of short periods of the SOI layer and a heat treatment utilizing a batch processing type furnace to improve the surface roughness of long periods of the SOI layer after the delamination step.

Applicants unexpectedly discovered that, if a wafer having an SOI layer is subjected to a heat treatment consisting of two stages utilizing separately a rapid heating/rapid cooling apparatus and a batch processing type furnace after the delamination as described above, surface crystallinity is restored and the surface roughness of both the short period and the long period are improved. Because this method does not use polishing such as touch polishing, thickness uniformity of the SOI layer is maintained.

Applicants found that a two-stage heat treatment can be performed by subjecting the wafers to a heat treatment in the rapid heating/rapid cooling apparatus and then a heat treatment in the batch processing type furnace. The surface roughness of short periods is improved by the heat treatment by the rapid heating/rapid cooling apparatus, and the surface roughness of long periods is improved by heat treatment utilizing the batch processing type furnace. Large quantities of wafers can be subjected to heat treatments at the same time in the batch processing type furnace, resulting in higher throughput than other methods in which wafers are subjected to a heat treatment for a long period of time by the single wafer processing in a rapid heating/rapid cooling apparatus. Accordingly, the short period components of surface roughness are improved within an extremely short period of time by the heat treatment using an RTA apparatus, and in addition, a lot of wafers can be processed at one time and the long period components are improved in a batch processing type furnace.

Importantly, the Applicants discovered for the first time that both the short period components and long period components of surface roughness are improved by the two-stage

heat treatment. In particular, Applicants unexpectedly discovered that, if the heat treatment in the rapid heating/rapid cooling apparatus for a short period of time is performed as the first stage, crystallinity of the surface is restored and COPs in the SOI layer are markedly reduced. When the heat treatment by the batch processing type furnace is performed in a subsequent stage, COPs in the SOI layer have already been substantially eliminated. Thus, Applicants unexpectedly discovered that even if a heat treatment using a batch processing type furnace is performed for a relatively long period of time, the etching of the buried oxide layer by hydrogen gas or argon gas and resultant pitting are suppressed.

Applicants have also unexpectedly found that an SOI wafer having improved surface roughness, uniform SOI layer thickness and being substantially free from COP-induced pits can be achieved by the method of independent claim 3. That is, Applicants found that an SOI wafer having improved surface roughness, uniform SOI layer thickness and being substantially free from COP-induced pits could be produced by the combination of:

- bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation, wherein an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on surface are reduced is used as the bond wafer;
- delaminating a wafer having an SOI layer at the micro bubble layer as a border,
- subjecting the wafer having an SOI layer to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace after the delamination step.

Applicants discovered for the first time that if an SOI wafer produced by using any one of an FZ wafer, an epitaxial wafer and a CZ wafer of which COPs at least on the surface are reduced is used as the bond wafer as described above, COPs in the SOI layer can be reduced or substantially completely eliminated. Reduction and elimination of COPs from the SOI layer reduces or eliminates etching of the buried oxide layer during heat treatments at

high temperatures for long periods of time in a batch processing type furnace. Thus, the surface roughness of the SOI layer can be reduced by heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace without producing pits of the buried oxide layer.

Thus, Applicants have discovered for the first time that heat treatments can be efficiently performed as a whole, and SOI wafers of superior surface characteristics can be produced at a low cost.

III. Rejections Under 35 U.S.C. §103(a)

Section 103 requires a consideration of the claimed invention as a whole and the prior art as a whole in making an obviousness determination. This involves considering the scope and content of the prior art, the differences between the prior art and the claims at issue, the level of ordinary skill in the art, and any secondary considerations that may be present. Graham v. John Deere, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966). Combination of references to support a rejection requires a motivation or suggestion in the art that one should carry out the claimed invention, and would have a reasonable expectation of success in doing so. In re Vaeck, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). Evidence of secondary considerations such as unexpected results, including such evidence in the specification, must be taken into account. MPEP §2144.08 II. A.

A. Claims 1 and 2 Are Patentable Over the Cited References

Claim 1 sets forth a "method for producing an SOI wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating a wafer having an SOI layer at the micro bubble layer as a border, wherein, after the delamination step, the wafer having an SOI layer is subjected, in an atmosphere containing hydrogen or argon, to both a heat treatment utilizing a rapid heating/rapid cooling apparatus

to improve the surface roughness of short periods of the SOI layer and a heat treatment utilizing a batch processing type furnace to improve the surface roughness of long periods of the SOI layer." Claim 2 depends from claim 1 and incorporates all the limitations of claim 1. As discussed in detail below, neither of the cited references, alone or in combination, teach or suggest the method of claim 1 or the beneficial results that proceed from this combination.

1. Yamamoto Does Not Teach or Suggest the Claimed Invention

Yamamoto is cited as disclosing a method for producing an SOI wafer by the hydrogen delamination method. The method disclosed by Yamamoto includes steps of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and delaminating the wafer. After the delamination step, Yamamoto discloses subjecting the wafer to RTA under hydrogen atmosphere to improve the surface roughness of the SOI layer.

However, claim 1 clearly includes the limitation that the wafer having an SOI layer be subjected to both a heat treatment utilizing a rapid heating/rapid cooling apparatus to improve the surface roughness of short periods of the SOI layer and a heat treatment utilizing a batch processing type furnace to improve the surface roughness of long periods of the SOI layer. This requirement reflects Applicants' discovery that RTA, such as the heat treatment in Yamamoto, improves only the short period components of surface roughness to a level comparable to that of mirror-polished wafers. The long period components of surface roughness are still inferior to mirror-polished wafers after RTA treatments. Applicants discovered, for the first time, that in order to improve the long period components of surface roughness, a heat treatment using high heat for a long period of time is required. As

Yamamoto performs a heat treatment in hydrogen atmosphere, but does not teach or suggest utilizing both a rapid heating/rapid cooling apparatus and a batch processing type furnace to improve both short periods and long periods of the SOI layer.

Thus, Yamamoto alone does not disclose, teach or suggest the invention of claims 1 and 2.

2. Sato Does Not Teach or Suggest the Claimed Invention

Sato is cited for its teachings of a semiconductor substrate, on which an insulating layer is formed and hydrogen ions are implanted, joining the semiconductor substrate to a support substrate and delamination the resulting structure. Sato is further cited as disclosing that after delamination, the structure is subjected to a heat treatment in a hydrogen annealing furnace.

Sato discloses the production of SOI wafers and that wafers having an SOI structure are set in a vertical-type hydrogen annealing furnace and subjected to a heat treatment in a hydrogen atmosphere for one to four hours at 1100°C. See Sato, paragraphs [0207] and [0273]. Thus, the Sato method only improves the surface roughness of long periods. The surface roughness of short periods, however, is not improved by the Sato process.

Although Sato performs a heat treatment in hydrogen atmosphere, Sato does not teach or suggest utilizing both a rapid heating/rapid cooling apparatus and a batch processing type furnace to improve both short periods and long periods of the SOI layer.

In addition, the Sato method does not produce an SOI wafer by the hydrogen ion delamination method, as described in claim 1. While the Office Action asserts that Sato discloses implanting hydrogen ions into a semiconductor surface, Sato itself makes clear that a substrate having a porous silicon layer is prepared by the anodization method using hydrofluoric acid, for example, and a nonporous microcrystalline layer is grown on the porous silicon layer, in which hydrogen ions are not implanted into the substrate. Sato's method is not a hydrogen ion delamination method, such as that described in claim 1. See Sato, paragraphs [0135]-[0138] and [0157]-[0158], Fig. 10A-10E and claims 1 and 2.

Thus, Sato alone does not disclose, teach or suggest the invention of claims 1 and 2.

3. Yamamoto and Sato Are Improperly Combined And Fail to Yield the Claimed Invention

The Office Action asserts that the combination of Yamamoto and Sato teaches annealing by either a furnace or RTA and that, for this reason, it would have been within the scope of one of ordinary skill in the art to use either RTA or furnace heating for the first heating step and the other for the second heating step, having a cooling step in between. Applicants respectfully disagree.

The method for producing an SOI wafer, as set forth in claim 1, clearly specifies that after the delamination step, the wafer having an SOI layer is subjected to a "two-stage heat treatment in an atmosphere containing hydrogen or argon utilizing a rapid heating/rapid cooling apparatus and a batch processing type furnace." Thus, Applicants submit that the language of the claims clearly indicates that the claimed method involves a two-stage heat treatment: one stage in an RTA apparatus and a second stage in a batch processing type furnace in an atmosphere containing hydrogen or argon. Applicants respectfully submit that neither of the cited references, either alone or in combination with each other, teaches or suggests a two-stage (two-type) heat treatment process as claimed.

Applicants respectfully submit that the Office Action is selectively combining only the heat treatment processes of Yamamato and Sato, without any motivation to do so. One of ordinary skill in the art would have understood that the surface roughness of the SOI layer could be improved by either hydrogen annealing using an RTA or hydrogen annealing using a batch-type furnace. However, without the knowledge or further investigation to discover that the surface roughness of short periods is improved by a rapid heating/rapid cooling apparatus and the surface roughness of long periods of the SOI layer is improved by a batch processing type furnace, even one of ordinary skill in the art would not have been motivated to selectively combine the heat treatments of Yamamoto and Sato. That is, because surface

roughness generally can be improved by either RTA or batch type furnaces, one of ordinary skill in the art would not have been motivated to perform two successive heat treatments in which two apparatuses of different types are required without a compelling reason to do so, at least because performing two heat treatments adds to the cost and time needed to perform a function apparently performed by one heat treatment.

Prior to Applicants' discoveries, it was unknown in the art that surface roughness of only short periods is improved by rapid heating/rapid cooling apparatus and the surface roughness of only long periods is improved by batch type furnaces. In particular, it was not known that neither type of heat treatment improves both the surface roughness of short and long periods of an SOI layer. None of the cited references disclose or suggest such a possibility. The art of record points to the need for only one heat treatment to improve surface roughness and does not contemplate the use of more than one heat treatment, or type of heat treatment. Thus, without a compelling reason, such as the knowledge provided by Applicants that surface roughness of short periods is improved by rapid heating/rapid cooling apparatus and the surface roughness of long periods is improved by batch type furnaces, such a process would not have been performed.

The Office Action asserts that in view of the individual teachings of the cited references, it would have been obvious to one of ordinary skill in the art to combine the teachings of Yamamoto with Sato to derive a two-stage heat treatment process as claimed. However, the Office Action has failed to provide any evidence to support that one of ordinary skill in the art would have been motivated to combine the teachings of the cited references as asserted.

Neither reference teaches or suggests that it would be desirable or advantageous to subject an SOI wafer to an additional heat treatment step, which would have required additional time and cost for no apparent reason. Although both references teach a heat

treatment to planarize a laminated surface, each reference only teaches or suggests a one-stage heat treatment. Neither reference teaches or suggests that an additional or subsequent heat treatment in the complementary apparatus would be desirable or advantageous.

In fact, each of Yamamoto and Sato appear to be directed to alternative methods for carrying out the same heat treatment process. Neither reference teaches or suggests that its disclosed process is deficient in any way, such that the disclosed process should be supplemented by a second heat treatment process. One of ordinary skill in the art, looking at the disclosures of Yamamoto and Sato, would not have been motivated to combine their separate teachings into a single, two-step process. Instead, one of ordinary skill in the art would only have been motivated to use either the process of Yamamoto or the process of Sato, since both are disclosed to be suitable and effective for their intended purpose.

At most, one of ordinary skill in the art might have been motivated to combine a heat treatment by an RTA apparatus and that by a batch processing type furnace into a single process by knowledge of the particular improvements to surface roughness provided by the different types of heat treatment. However, this knowledge was disclosed for the first time in the present application. There is no motivation to utilize both a rapid heating/rapid cooling apparatus and a batch type furnace in a single process in either of the cited references. different.

Clearly, the only motivation for combining the cited references comes from a hindsight reconstruction of the claimed invention. The Office Action has based the rejection solely on picking and choosing the instant claim limitations from two cited references.

It has clearly been held that the reason, suggestion or motivation for combining the references "can not come from the applicant's invention itself." In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). That is, the motivation for combining the references can not be

a product of hindsight reconstruction of the claimed invention based on applicant's own disclosure. Such a hindsight reconstruction has clearly been made in the present Office Action.

The Office Action asserts that the claimed invention would have been obvious based on a hindsight selection of the claimed limitations, as evidenced by the teachings of the cited references, neither of which would suggest to one skilled in the art that the teachings could or should be combined and then further modified to provide the claimed invention. Such a combination is improper because the references, viewed by themselves and not in retrospect, must suggest the combination asserted by the Office Action. In re Shaffer, 229 F.2d 476, 108 USPQ 326 (C.C.P.A. 1956); In re Stoll, 523 F.2d 1392, 187 USPQ 481 (C.C.P.A. 1975).

As discussed above, the references do not provide any motivation for combining the separately disclosed heat treatment processes. Sato discloses hydrogen annealing to improve surface roughness. Yamamoto discloses that surface roughness may be improved by heat treatment using either RTA or a batch processing type furnace. Each reference teaches a single heat treatment. Neither reference teaches or suggests that an additional or subsequent heat treatment in the complementary apparatus would be desirable or advantageous.

In addition, it is impermissible within the framework of 35 U.S.C. §103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation that the reference fairly suggests to one of ordinary skill in the art. In re Wesslau, 147 USPQ 391, 393 (CCPA 1965). The Office Action apparently takes the position that the teaching of different types of heat treatments for the same purpose, without additional motivation, is sufficient to support combining Yamamoto and Sato to arrive at the two-stage heat treatment of claim 1. However, both references teach only the use of one heat treatment; neither reference suggests a two-stage treatment. The Office Action thus is impermissibly picking and choosing claim limitations from the references, without consideration of the teachings of the references as a whole.

Furthermore, neither reference teaches or suggests that the surface roughness of both long and short periods may be improved by subjecting the SOI wafers to a two-stage heat treatment process. As stated in the specification, at page 8, lines 1-11, "surface crystallinity is restored and the surface roughness of short periods is improved in the heat treatment by the rapid heating/rapid cooling apparatus, and the surface roughness of long periods can be improved by the heat treatment utilizing the batch processing type furnace." Thus, the treatment of the SOI wafers under different conditions in two different apparatus yields results that would not be attainable using the methods described in the cited references because the references only teach the use of individual, alternative heat treatment processes. As such, these results would have been unexpected over the teachings of Yamamoto and Sato.

The only motivation for combining the cited references in the manner asserted in the Office Action derives from the disclosure of the present application, which is clearly improper.

Accordingly, one of ordinary skill in the art would not have been motivated to perform a two-stage heat treatment by utilizing two different types of heat treatment apparatus, as set forth in claim 1.

Further, the Sato method differs completely from the hydrogen ion delamination method of claim 1 and the hydrogen ion delamination method of Yamamoto. Accordingly, there is no motivation in either Sato or Yamamoto to combine only a heat treatment for a wafer after forming an SOI wafer by the method of Sato with the heat treatment of Yamamoto, or vice versa, to produce an SOI wafer since the methods are completely different from each other.

For at least these reasons, Yamamoto and Sato, alone or in combination, do not teach or suggest the invention of claims 1 and 2. Accordingly, reconsideration and withdrawal of this rejection are requested.

B. Claim 3 Is Patentable Over the Cited References

Claim 3 sets forth a "method for producing an SOI wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating a wafer having an SOI layer at the micro bubble layer as a border, wherein an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on surface are reduced is used as the bond wafer, and the wafer having an SOI layer is subjected to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace after the delamination step." As discussed in detail below, neither of the cited references, alone or in combination, teach or suggest the method of claim 3 or the beneficial results that proceed from this combination.

When a normal CZ wafer is used as the bond layer of the SOI wafer, pits of the buried oxide layer are formed by etching through COPs in the SOI layer during the hydrogen annealing treatment. See, for example, Specification, page 4, line 12 - page 5, line 7; page 6, line 24 - page 7, line 3. As disclosed in the instant specification and discussed above, Applicants discovered, for the first time, that if an SOI wafer produced by using any one of an FZ wafer, an epitaxial wafer and a CZ wafer of which COPs at least on the surface are reduced is used as the bond wafer as described above, COPs in the SOI layer can be reduced or substantially completely eliminated. Etching of the buried oxide layer can be reduced or eliminated by the reduction and elimination of COPs from the SOI. Thus, the surface roughness of the SOI layer can be reduced by heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace without producing pits of the buried oxide layer.

Applicants discovered that if a wafer without COPs or whose COPs are reduced is used as a bond wafer, as in claim 3, the COPs in SOI layer can be reduced or substantially

eliminated, etching of the buried oxide layer due to COPs is not caused, and a heat treatment at a high temperature for a long period of time in a batch processing type furnace becomes possible. See Specification, page 10, lines 3-12, and page 11, lines 12-18. That is, it is possible to perform heat treatments in batch processing type furnaces without etching the buried oxide layer. Thus, by using a CZ wafer in which the grown-in defects, such as COPs are reduced, an SOI wafer having good surface roughness in both long and short periods can be obtained.

Specifically and as disclosed in the specification, SOI wafers are produced by using as a bond wafer a CZ wafer produced from a single crystal ingot of which grown-in defects, such as COPs, are reduced for the whole crystal by controlling V/G (V: pulling rate, G: temperature gradient along the direction of solid-liquid interface of crystal) (see, for example, Example 3), or an epitaxial wafer (see, for example, Example 4), respectively, and then are subjected to a heat treatment utilizing a batch processing type furnace. See Specification, page 40, line 27 - page 43; Table 3. Consequently, the surface roughness for both 1 μm square (short periods) and 10 μm square (long periods) are improved up to the same level as Examples 1 and 2 corresponding to claims 1 and 2. See Specification, Table 2. By producing an SOI wafer by using the wafer recited in claim 3 as a bond wafer, and after the delamination, performing a heat treatment in the atmosphere containing hydrogen or argon, generation of pits due to COPs can be prevented and a surface roughness for both short and long periods can be sufficiently improved. None of the cited references disclose, teach or suggest using a wafer having reduced COPs as the bond wafer for producing an SOI wafer by hydrogen ion delamination.

1. **Yamamoto and Sato Fail to Have Rendered Obvious the Claimed Invention**

The Office Action applies Yamamoto and Sato to claim 3 in the same way the references were applied to claims 1 and 2, discussed in detail above. Yamamoto and Sato, alone or in combination, do not disclose, teach or suggest the invention of claim 3 for at least the same reasons as discussed with reference to claims 1 and 2. The deficiencies of Yamamoto and Sato are not remedied by Adachi and Wolf.

Because the rejection relies on the combination of Yamamoto and Sato as the primary references, Applicants respectfully submit that the rejection should be withdrawn. Even if one of ordinary skill in the art were to combine the teachings of Adachi and Wolf with those of Yamamoto and Sato, the citation of Adachi and Wolf fails to cure the deficiencies identified in the teachings of Yamamoto and Sato for the reasons discussed above.

2. **All Four Cited References Fail to Yield the Claimed Invention**

Wolf generally teaches the subjects of silicon single crystal growth and wafer preparation. Wolf teaches wafer preparation from silicon single crystals grown by both the Czochralski and Floating Zone methods. Wolf is cited only for its disclosure of general wafer preparation from Czochralski silicon single crystals.

Adachi was cited as disclosing a Czochralski silicon single crystal bond wafer, in which the COPs on at least the surface have been reduced. Adachi discloses that wafers stacked up as shown in Fig. 1b are annealed in a furnace so that grown-in defects, which give rise to surface COP and internal COP, are eliminated. See Adachi, col. 1, lines 25-33.

The Office Action suggests that it would have been within the scope of one of ordinary skill in the art to use the Adachi CZ wafer as the bond wafer and thus enhance the quality of the finished product. Applicants respectfully disagree with the Office Action's conclusions.

Adachi teaches that wafers are annealed in a furnace to eliminate grown in defects, which give rise to surface and internal crystal originated particles (COP). Wolf discloses general wafer preparation from Czochralski silicon single crystals.

However, contrary to the assertion of the Office Action, one of ordinary skill in the art would not have been motivated to combine the teachings of Adachi with those of Yamamoto and Sato. None of the references teaches or suggests that a CZ wafer in which COPs on the surface are reduced should be used as a bond wafer because none of the references recognize that a buried oxide layer is etched through COP by hydrogen gas. Thus, one of ordinary skill in the art would not have been motivated to combine the teachings of Adachi with the cited primary references.

In contrast to claim 3, none of the cited references disclose, teach or suggest that the buried oxide layer is etched through COPs in the SOI layer when the SOI wafer after the delamination is subjected to heat treatment in the atmosphere containing hydrogen or argon. Likewise, none of the cited references teach or suggest a solution to this problem, or any motivation to combine these references to solve the unspecified problem.

None of the references disclose, teach or suggest that generation of pits can be prevented, and none of the references disclose, teach or suggest that a surface roughness for both short and long periods can be sufficiently improved by employing a bond wafer whose COPs in an SOI layer are reduced, and performing a heat treatment in the atmosphere containing hydrogen or argon. Thus, there is no motivation or suggestion in the cited references to use an Adachi CZ wafer as the bond wafer. One of ordinary skill in the art would not have been motivated to combine or modify these references to derive the subject matter of claim 3, and the cited references, alone or in combination, do not disclose, teach or suggest the subject matter of claim 3.

Thus, Yamamoto, Sato, Adachi and Wolf, alone or in combination, would not have rendered claim 3 obvious. Accordingly, reconsideration and withdrawal of this rejection is requested.

C. Conclusion

Considered in light of all of the factors relevant to an obviousness determination, Yamamoto, Sato, Adachi and Wolf, alone and together, do not teach or suggest the claimed combination or the unexpected results achieved thereby. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-3, and dependent claims 6-8, are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

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